Attorney's Docket No.: 10559-270001
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Applicant: Overkamp et al.
Serial No.: 09/675,816
Filed: September 28, 2000

Art Unit: 2183
Examiner: Charles A. Harkness

Title : Digital Signal Processor With Multiple Instruction Destinations For A Pipelined System

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attached to this facsimile communication cover sheet is Response to Notification of Non-Compliant Appeal Brief and Rebusmission of Appeal Brief faxed this 25th day of February, 2005, to the United States Patent and Trademark Office.

Respectfully submitted,

Date: February 25, 2005

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Attorney's Docket No.: 10559-270001/P9277 - ADI APD1796-1-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gregory A. Overkamp et al. Art Unit: 2183
Serial No.: 09/675,816 Examiner: Charles A. Harkness
Filed : September 28, 2000
Title : DIGITAL SIGNAL PROCESSOR WITH MULTIPLE INSTRUCTION DESTINATIONS FOR A PIPELINED SYSTEM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF AND RESUBMISSION OF APPEAL BRIEF

Sir:

Applicant herewith resubmits the brief on appeal originally filed on October 30, 2004, including a rewritten concise explanation/summary of claimed subject matter, as requested by the notification in paper number 2005 0119.

Respectfully submitted,

Date: 2/25/05

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Attorney's Docket No.: 10559-270001 / P9277 - ADI APD1796-1-US

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BRIEF ON APPEAL

Sir:

Applicant herewith files this brief on appeal, thereby perfecting the Notice of Appeal that was originally filed on July 20, 2004. The sections required by the rules follow:

(1) Real Party in Interest

The application is assigned of record to Intel Corp., and Analog Devices Inc., who are jointly the real party in interest.

(2) Related Appeals and Interferences

There are no known related appeals and/or interferences.

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

October 20, 2004
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Brenda Lewis
Typed or Printed Name of Person Signing Certificate

(3) Status of Claims

Claims 1, 3-5, 7-8, 10-18 are pending. Each of these claims are rejected, and each of these claims are correspondingly appealed.

(4) Status of Amendments

A request for reconsideration was filed on June 1, 2004. The request for reconsideration was indicated as having been considered.

(5) Summary of Claimed Subject Matter

The present system relates to a partial instruction decoding and re-encoding, for example for use in a signal processor. According to the present claims, different instructions may be broken into different parts and sent to different places. Claim 1 requires decoding a portion of the instruction to determine first and second destinations. This is described in the specification for example page 10 beginning at line 11. Page 10, line 21 describes that the decoder may decode either the entire instruction or only a part of the instruction. Those instructions are used to modify the registers, see for example page 11,lines 1-5. If portions of the instructions are to be sent to the system pipe, then those instructions are re-

encoded. See for example page 11, line 14, covered by claim 1's step of "re-encoding only a portion of the instruction...". The remaining portion, which is not re-encoded, can be used for other functions. See for example page 11, lines 19-21.

According to this system, therefore, only a part of the instruction needs to be decoded and re-encoded.

Claim 8 defines a processor instruction, and determining the first functional unit which operates based on the coded instructions and a second functional unit which operates based on the decoded information, as well as a third functional unit. Page 9 describes the procedure carried out in this way. The bottom of page 9 describes that the instruction may be sent to the execute unit to be executed without decoding. Page 10, lines 11-21, describes that a portion of the instruction may be sent to the data address generator, and decoded before being sent to that generator. Other parts of the instruction may also be sent to other portions, see generally, page 11 lines 6-21.

Claim 8 defines forwarding a first portion to a first destination as described above, decoding another portion and forwarding that other portion as described above. Any remaining portion may be encoded to a second code, see generally page 11 lines 19-21, and the encoded instructions may be sent to a third functional unit see page 11 lines 22-23.

Claim 14 defines a processor which includes a decoder and an encoder. Again, the processor generally shown as 110 in figure 1 operates according to figure 5. The processor decoder decodes the instruction to determine the destination; see generally page 9 lines 13-20.

A portion of the instruction is sent to the first destination which operates on that decoded code. See generally page 10 beginning line 21. Some of these portions may be re-encoded, see generally page 11 lines 11-15, and used for a second destination, see generally page 11 lines 22-23.

(6) Grounds Of Rejection To Be Reviewed On Appeal

In the final rejection, all of the pending claims were rejected under 35 USC 102 as allegedly being anticipated by the Hennessy reference. The question on appeal is whether these claims are properly rejected as being anticipated by Hennessy.

(7) Argument

The Hennessy reference, as applied by the patent office, is actually only a single figure, with minimal explanation, figure 5.48. For reasons set forth herein, it is respectfully suggested that the Hennessy reference does not meet the patent

office's burden of providing a prima facie showing of unpatentability.

First, the rejection states that Hennessy determines the kind of instruction from the opcode. The rejection states that Hennessy forwards signals based on the kind of instructions that are present. The rejection labels the first destination as Hennessy's ALU, and the second destination as the registers.

With all due respect, this attempts to read more into Hennessy than is actually there. Claim 1 requires decoding at least a portion of an instruction "to determine a first destination and a second destination of the instruction". Nothing in the single figure in any way suggests this dual destination feature. In the response to arguments, attached as part of the advisory action paper number 2004 0709, the rejection states that "some of the outputs go to registers after passing through muxes and some outputs go directly to a mux and then on to the ALU, after the mux has determined which outputs should be directed onto the associated destination." Therefore Hennessy has taught determining which outputs will go to certain destinations." With all due respect, however, this paraphrases the claim and does not find the claimed limitation in the prior art. Claim 1 requires decoding a portion of the instruction to determine the first destination and the second destination of

the instruction. That is, the destinations must be determined from decoding a portion of the instruction according to this claim.

By the patent office's own admission, at best, the mux makes the decision in Hennessy. The rejection uses a lot of supposition in determining what Hennessy does. However, even assuming arguendo that the Examiner's interpretation of how Hennessy works is correct, it only shows that the muxes select which outputs are directed to which destinations. It shows nothing about the determination being made by decoding a portion of an instruction. And in fact, Hennessy's single figure certainly shows nothing about decoding at least a portion of an instruction to determine the first and second destinations as claimed. One could suppose that that might be one possibility of what Hennessy might be doing. However, there is certainly no actual teaching of doing so in Hennessey. For these reasons, that rejection does not meet the patent office's burden of providing a prima facie showing of unpatentability.

Claim 1 also requires re-encoding only a portion of the instruction and forwarding that re-encoded instruction to the first destination. The rejection states that the control unit in Hennessy "has to" both decode the opcode to determine what kind of instruction exists, and also "the control instructions

to be sent to operate the ALU control". With all due respect, this is based on hindsight, and not on Hennessy's teaching. Nowhere is there any suggestion in Hennessy that supports this postulate of what is inherently occurring. In fact, it is believed that the rejection can only conclude that this is inherently occurring, because of the teaching of the present specification. Nowhere is there any teaching or suggestion of re-encoding any control instruction whatsoever, much less re-encoding only a portion of the instruction, as claimed. Presumably the instruction register in Hennessy carries out any control which is necessary based on the opcode. There is no teaching of re-encoding.

Claim 1 also requires forwarding a different portion, without re-encoding, to the second destination. The rejection alleges that some outputs are not re-encoded. However, and with all due respect again, many of the instructions go to the same places, to the registers and the ALU's. There is quite simply no teaching or suggestion that one portion of the instruction is re-encoded and another portion of the instruction is not re-encoded. The entire rejection is simply a speculation on what Hennessy might be doing. Therefore, claim 1 should be allowable for these reasons, along with the claims which depend therefrom.

Claim 8 requires receiving a coded processor instruction, determining functional units, one of which operates based on coded instructions, one of which operates based on decoded information, and a third unit; each of which receive parts of the instructions, and forwarding the instructions to those units. One of the operations requires re-encoding any remaining portion to a second code and forwarding that re-encoded instruction to a third location. As described above, there is no teaching or suggestion of the re-encoding in Hennessy, and the single figure does not meet the patent office's burden of providing a prima facie showing of unpatentability. Therefore, claim 8 should be allowable along with claims 10-13 which depend therefrom.

Claim 14 requires a decoder, and an encoder, where the decoder decodes at least a portion to determine a first destination and a second destination, forwards a portion of the instruction to the first destination, and the encoder re-encodes a portion of the instruction used for the second destination. As described above, this is in no way taught or suggested by the cited prior art.

Finally, to correct the statement made in the amendment after final in the previous amendment, the remarks stated that all of the outputs from the instruction register went to the

register and into the ALU. In retrospect, however, it appears that certain parts of the instruction (31-26) actually go to the control, not to the register. In any case, it is respectfully suggested that the rejection does not meet the patent office's burden for the above reasons.

For reasons stated above, the examiner's rejection should be reversed.

Applicant hereby petitions under 37 C.F.R. §1.136 for a 1 month extension of time. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: February 25, 2005

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Appendix: All claims on appeal.
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Appendix of Claims

1. A method of handling instructions within a processor comprising:

decoding at least a portion of an instruction to determine a first destination and a second destination of the instruction;

re-encoding only a portion of the instruction to a second re-encoded code used for said first destination and forwarding the re-encoded instruction to said first destination; and

forwarding a different portion of the instruction, without re-encoding, to said second destination.

3. The method of Claim 1, wherein said first destination is a first functional unit which operates based on op codes.

4. The method of Claim 3, further comprising sending at least a portion of the decoded instruction to a second functional unit which operates based on decoded information.

5. The method of Claim 1, further comprising determining a portion of the coded instruction to decode.

7. The method of Claim 1, further comprising handling instructions in a digital signal processor.

8. A method of processing instructions within a processor comprising:

receiving a coded processor instruction;

determining a first functional unit which operates based on coded instructions, a second functional unit which operates based on decoded information obtained from the coded instruction, and a third functional unit, which each receive parts of the instruction;

forwarding a first portion of the coded instruction having a first destination location representing the first functional unit, to the first functional unit;

decoding another portion of the instruction;

forwarding said another portion of the decoded instruction having a second destination location representing the second functional unit, to the second functional unit;

re-encoding any remaining portion of the instruction to a second code; and

forwarding the re-encoded instruction to a third location representing the third functional unit.

10. The method of Claim 8, wherein said second functional unit is a data address generator.

11. The method of Claim 8, wherein the third functional unit is a system pipe.

12. The method of Claim 8, further comprising processing instructions within a digital signal processor.

13. The method of Claim 8, further comprising decoding and re-encoding with a decoder.

14. A processor comprising:

a decoder which receives an instruction coded in a first code and decodes at least a portion of the instruction to determine a first destination and a second destination of the instruction and forwards a portion of the instruction to said first destination, which operates based on a decoded code;

an encoder which re-encodes a portion of the instruction to a second encoded code used for said second destination.

15. The processor of Claim 14, wherein the decoder determines the destination of the instruction.

16. The processor of Claim 15, wherein the decoder forwards control signals to other portions of the processor.

17. The processor of Claim 16, wherein the control signals may be in the first code or the second code.

18. The processor of Claim 14, wherein the processor is a digital signal processor.